Tertiary Infotech Academy
Course Development | Training | Agentic AI Automation

Course Code: **C420**

Verilog Programming Training for FPGA

COURSE INFORMATION

Sessions	Duration	Level	Assessment
2 days	15 hrs	Intermediate	NA

VENUE

12 Woodlands Square #07-85/86/87 Woods Square Tower 1, Singapore 737715. 5 mins walk from Woodlands (NS9) MRT station.

The venue is disabled-friendly.

WHAT'S THIS COURSE ABOUT

FPGA Design FLOW

Motivation

Topic 1 : Architecture of FPGA

Introduction to Programmable logic device (PLD)

Architecture

Structure of PLD

Topic 2 : Introduction to Verilog

Levels of Abstraction

Syntax & Semantics

Reserved Keywords

Topic 3: Verilog Ports

Ports declaration

Data types

Physical

Abstract

Constant

Topic 4: Operators

Arithmetic Operator

Bit Wise

Logical

Reduction

Shift

Relational/Equality/Concatenation/Replication/Conditional

Topic 5...

COURSE FEE

Full Fee S$600.00 Before GST	GST S$54.00 9% of fee
Total Payable S$654.00 Including GST	

CERTIFICATION

- **Certificate of Completion from Tertiary Infotech** - Upon meeting at least 75% attendance and passing the assessment(s), participants will receive a Certificate of Completion from Tertiary Infotech.

REGISTRATION

https://www.tertiarycourses.com.sg/verilog-programming-training-for-fpga.html

SCAN TO REGISTER

SUPPORT

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